IN THE CLAIMS

1. (Currently Amended) A method to provide a triple well in an epitaxially based CMOS or BiCMOS process, comprising the step of implanting the triple **using arsenic** well prior to the epitaxial deposition **wherein a slow diffusion will occur, and implanting Boron prior to the epitaxial deposition**.

2. (Cancelled).

3. (Cancelled) .

4. (Cancelled) .

5. (Cancelled)

6. (Currently Amended) The method according to claim **[4]1**, comprising the step of adding more than one NMOS device in an achieved structure.

7. (Currently Amended) The method according to claim **[5]21**, comprising the step of adding more than one NMOS device in an achieved structure.

8. (Currently Amended) A method to provide a triple well in an epitaxially based CMOS or BiCMOS process, comprising the steps of:

- providing a semiconductor substrate;
- applying a first mask having openings only in areas for said triple well;
- applying an ion implant;
- applying a second mask having openings surrounding said ion implant;
- implanting a first area surrounding said ion implant;
- depositing an epitaxial layer,
- **providing a third mask on top of said substrate before depositing said epitaxial layer, and**
- **implanting at least a second area**.

9. (Original) The method according to claim 8, wherein the ion implant is an arsenic ion implant.

10. (Original) The method according to claim 8, wherein a doping dose of $2x10^{13}$ cm^{-2}, energy of 480 keV and a tilt angle of 0 degree is used to penetrate deep into the substrate.

11. (Cancelled).

12. (Cancelled).

13. (Currently Amended) The method according to claim **[12]22**, wherein the third areas are filled by a dielectric material.

14. (Original) The method according to claim 13, wherein the dielectric material is a High Density Plasma oxide.

15. (Currently Amended) The method according to claim **[11]8**, further comprising the step of etching said epitaxial layer to provide third areas above said first and second trenches.

16. (Previously Presented) The method according to claim 15, wherein the third areas are filled by a dielectric material.

17. (Original) The method according to claim 16, wherein the dielectric material is a High Density Plasma oxide.

18. (Currently Amended) The method according to claim **[12]22**, further comprising the step of planarizing said epitaxial layer.

19. (Original) The method according to claim 18, wherein the planarizing is performed by chemical and/or mechanical polishing.

20. (Previously Presented) The method according to claim 8, wherein the substrate is of p-type and the triple well and first areas are of n-type.

21. (NEW) A method to provide a triple well in an epitaxially based CMOS or BiCMOS process, comprising the step of implanting the triple well prior to the epitaxial deposition, implanting Boron prior to the epitaxial deposition, and adding at least one NMOS device in an achieved structure.

22. (NEW) A method to provide a triple well in an epitaxially based CMOS or BiCMOS process, comprising the steps of:

- providing a semiconductor substrate;
- applying a first mask having openings only in areas for said triple well;
- applying an ion implant;
- applying a second mask having openings surrounding said ion implant;
- implanting a first area surrounding said ion implant;
- depositing an epitaxial layer; and
- etching said epitaxial layer to provide third areas above said first areas.